

**INFORMATION DISCLOSURE
STATEMENT BY APPLICANTS
PTO-1449**

Attorney Docket No.
2885/93

Serial No.
10/523,764

Applicant(s)
Vorbach et al.

Filing Date
August 2, 2005

Group Art Unit
2187

U.S. PATENT DOCUMENTS

EXAMINER'S INITIALS	PATENT/ PUBLICATION NUMBER	PATENT/PUBLICATION DATE	NAME	CLASS	SUBCLASS	FILING DATE
/T.T./	RE34,444	November 1993	Kaplinsky			
	RE37,195	May 29, 2001	Kean			
	4,414,547	November 1983	Knapp et al.			
	4,590,583	May 20, 1986	Miller			
	4,667,190	May 1987	Fant et al.			
	4,882,687	November 1989	Gordon			
	4,884,231	November 1980	Mor et al.			
	4,918,440	April 17, 1990	Furtek et al.			
	4,972,314	November 1990	Getzinger et al.			
	5,010,401	April 1991	Murakami et al.			
	5,034,914	July 1991	Osterlund			
	5,041,924	August 1991	Blackborow et al.			
	5,099,447	March 1992	Myszewski			
	5,193,202	March 1993	Jackson et al.			
	5,212,716	May 1993	Ferraiolo et al.			
	5,218,302	June 8, 1993	Loewe et al.			
	5,237,686	August 1993	Asano et al.			
	5,276,836	January 4, 1994	Fukumaru et al.			
	5,327,125	July 1994	Iwase et al.			
	5,343,406	Aug 30, 1994	Freeman et al.			
	5,418,953	May 1995	Hunt et al.			
	5,469,003	November 1995	Kean			
	5,537,580	July 1996	Giomi et al.			
	5,550,782	Aug 27, 1996	Cliff et al.			
	5,581,731	December 3, 1996	King et al.			
	5,625,836	Apr 29, 1997	Barker et al.			
	5,646,544	Jul 8, 1997	Iadanza			
	5,646,545	Jul 8, 1997	Trimberger et al.			
	5,652,529	July 1997	Gould et al.			
	5,737,565	April 1998	Mayfield			
	5,748,979	May 1998	Trimberger			
	5,752,035	May 1998	Trimberger			
	5,754,459	May 19, 1998	Telikepalli			
	5,754,820	May 19, 1998	Yamagami			
	5,781,756	Jul 14, 1998	Hung			
	5,781,756	Jul 14, 1998	Hung			
	5,801,547	September 1, 1998	Kean			
/T.T./	5,801,958	September 1998	Dangelo et al.			

**INFORMATION DISCLOSURE
STATEMENT BY APPLICANTS
PTO-1449**

Attorney Docket No.
2885/93

Serial No.
10/523,764

Applicant(s)
Vorbach et al.

Filing Date
August 2, 2005

Group Art Unit
2187

EXAMINER'S INITIALS	PATENT/ PUBLICATION NUMBER	PATENT/PUBLICATION DATE	NAME	CLASS	SUBCLASS	FILING DATE
T.T./	5,815,715	September 1998	Kayhan			
	5,821,774	October 1998	Veytsman et al.			
	5,831,448	Nov 3, 1998	Kean			
	5,844,422	December 1, 1998	Trimberger et al.			
	5,857,097	January 1999	Henzinger et al.			
	5,862,403	January 1999	Kanai et al.			
	5,870,620	Feb 9, 1999	Kadosumi et al.			
	5,889,533	Mar 30, 1999	Lee			
	5,933,023	Aug 3, 1999	Young			
	5,960,193	September 28, 1999	Gutttag et al.			
	5,966,143	Oct 12, 1999	Breternitz, Jr.			
	5,978,583	November 1999	Ekanadham et al.			
	5,999,990	December 1999	Shamit et al.			
	6,020,760	February 1, 2000	Sample et al.			
	6,026,481	February 2000	New et al.			
	6,044,030	Mar 28, 2000	Zheng et al.			
	6,077,315	June 2000	Greenbaum et a.			
	6,084,429	July 2000	Trimberger			
	6,105,106	August 2000	Manning			
	6,134,166	October 17, 2000	Lytle et al.			
	6,137,307	October 2000	Iwanczuk et al.			
	6,154,048	November 2000	Iwanczuk et al.			
	6,154,049	Nov 28, 2000	New			
	6,157,214	December 5, 2000	Marshall			
	6,185,256	February 2001	Saito et al.			
	6,185,731	February 2001	Maeda et al.			
	6,188,240	February 2001	Nakaya			
	6,198,304	March 2001	Sasaki			
	6,201,406	March 2001	Iwanczuk et al.			
	6,204,687	March 2001	Schultz et al.			
	6,215,326	April 10, 2001	Jefferson et al.			
	6,216,223	April 2001	Revilla et al.			
	6,252,792	June 26, 2001	Marshall et al.			
	6,256,724	July 2001	Hocevar et al.			
	6,262,908	July 17, 2001	Marshall et al.			
	6,266,760	July 2001	DeHon et al.			
	6,285,624	September 2001	Chen			
	6,311,265	October 2001	Beckerle et al.			
T.T./	6,353,841	March 5, 2002	Marshall et al.			

**INFORMATION DISCLOSURE
STATEMENT BY APPLICANTS
PTO-1449**

Attorney Docket No.
2885/93

Serial No.
10/523,764

Applicant(s)
Vorbach et al.

Filing Date
August 2, 2005

Group Art Unit
2187

EXAMINER'S INITIALS	PATENT/ PUBLICATION NUMBER	PATENT/PUBLICATION DATE	NAME	CLASS	SUBCLASS	FILING DATE
/T.T./	6,362,650	Mar 26, 2002	New et al.			
	6,374,286	April 2002	Gee			
	6,373,779	Apr 16, 2002	Pang et al.			
	6,381,624	April 2002	Colon-Bonet et al.			
	6,400,601	June 2002	Sudo et al.			
	6,421,808	July 2002	McGeer			
	6,421,809	July 2002	Wuytack et al.			
	6,425,054	July 23, 2002	Nguyen			
	6,427,156	Jul 30, 2002	Chapman et al.			
	6,430,309	August 2002	Pressman et al.			
	6,434,642	Aug 13, 2002	Camilleri et al.			
	6,434,699	August 13, 2002	Jones et al.			
	6,435,054	October 10, 2000	Nguyen			
	6,438,747	August 2002	Schreiber et al.			
	6,476,634	November 2002	Bilski			
	6,487,709	November 2002	Keller et al.			
	6,490,695	December 2002	Zagorski et al.			
	6,507,947	January 2003	Schreiber et al.			
	6,516,382	February 2003	Manning			
	6,518,787	February 2003	Allegretti et al.			
	6,523,107	February 18, 2003	Stansfield et al.			
	6,525,678	February 2003	Veenstra et al.			
	6,539,415	March 25, 2003	Mercs			
	6,539,438	March 25, 2003	Ledzius et al.			
	6,542,394	April 1, 2003	Marshall et al.			
	6,542,844	April 2003	Hanna			
	6,553,395	April 22, 2003	Marshall et al.			
	6,567,834	May 20, 2003	Marshall et al.			
	6,631,487	October 2003	Abramovici et al.			
	6,633,181	October 2003	Rupp			
	6,658,564	December 2003	Smith et al.			
	6,708,325	March 2004	Cooke et al.			
	6,754,805	June 2004	Yujen Juan			
	6,757,847	June 2004	Farkash et al.			
/T.T./	6,757,892	June 2004	Gokhale et al.			

**INFORMATION DISCLOSURE
STATEMENT BY APPLICANTS
PTO-1449**

Attorney Docket No.
2885/93

Serial No.
10/523,764

Applicant(s)
Vorbach et al.

Filing Date
August 2, 2005

Group Art Unit
2187

EXAMINER'S INITIALS	PATENT/ PUBLICATION NUMBER	PATENT/PUBLICATION DATE	NAME	CLASS	SUBCLASS	FILING DATE
/T.T./	6,782,445	August 2004	Olgiati et al.			
	6,785,826	August 31, 2004	Durham et al.			
	6,802,206	October 2004	Patterson et al.			
	6,803,787	October 2004	Wicker, Jr.			
	6,820,188	November 16, 2004	Stansfield et al.			
	6,829,697	December 2004	Davis et al.			
	6,847,370	January 2005	Baldwin et al.			
	6,871,341	March 2005	Shyr			
	6,874,108	March 2005	Abramovici et al.			
	6,886,092	April 2005	Douglass et al.			
	6,901,502	May 2005	Yano et al.			
	6,961,924	November 2005	Bates et al.			
	6,928,523	August 2005	Yamada, Akira			
	6,977,649	December 2005	Baldwin et al.			
	7,000,161	February 2006	Allen et al.			
	7,007,096	February 2006	Lisitsa et al.			
	7,010,687	March 2006	Ichimura			
	7,038,952	May 2, 2006	Zack et al.			
	7,210,129	April 2007	May et al.			
	7,237,087	June 26, 2007	Vorbach et al.			
	7,249,351	July 2007	Songer et al.			
	7,254,649	August 2007	Subramanian et al.			
	7,340,596	March 2008	Crosland et al.			
	7,350,178	March 2008	Crosland et al.			
	2001/001860	May 2001	Bieu			
	2001/010074	July 26, 2001	Nishihara et al.			
	2001/032305	October 2001	Barry			
	2002/083308	June 27, 2002	Pereira et al.			
	2002/103839	August 2002	Ozawa			
	2002/124238	September 05, 2002	Metzgen			
	2002/138716	September 26, 2002	Master et al.			
	2003/001615	January 2003	Sueyoshi et al.			
	2003/061542	March 2003	Bates et al.			
	2003/062922	Apr 3, 2003	Douglass et al.			
/T.T./	2003/086300	May 2003	Noyes et al.			

INFORMATION DISCLOSURE STATEMENT BY APPLICANTS PTO-1449	Attorney Docket No. 2885/93	Serial No. 10/523,764
	Applicant(s) Vorbach et al.	
	Filing Date August 2, 2005	Group Art Unit 2187

EXAMINER'S INITIALS	PATENT/ PUBLICATION NUMBER	PATENT/PUBLICATION DATE	NAME	CLASS	SUBCLASS	FILING DATE
/T.T./	2005/066213	March 2005	Vorbach et al.			
↓	2005/0144210	Jun 30, 2005	Simkins et al.			
	2005/0144212	Jun 30, 2005	Simkins et al.			
	2005/0144215	Jun 30, 2005	Simkins et al.			
	2006/0130096	Oct 12, 2006	Thendean et al.			
/T.T./	2006/0230094	Oct 12, 2006	Simkins et al.			

FOREIGN PATENT DOCUMENTS

EXAMINER'S INITIALS	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATION	
						YES	NO
/T.T./	0 398 552	November 22, 1990	EPO				
↓	0 746 106	December 4, 1996	EPO				
	1 061 439	December 20, 2000	EPO				
	1 669 885	Jun 14, 2006	EPO			Abstract	
	WO92/001987	February 6, 1992	PCT				
	WO98/010517	March 12, 1998	PCT				
	WO98/035294	August 13, 1998	PCT				
	WO00/049496	August 24, 2000	PCT				
	WO00/077652	December 21, 2000	PCT				
	WO02/050665	June 27, 2002	PCT				
	WO02/071196	September 12, 2002	PCT				
	WO04/114128	December 29, 2004	PCT				
	WO04/053718	June 24, 2004	PCT				
	WO05/045692	May 19, 2005	PCT				
	08069447	March 12, 1996	Japan			Abstract	
	2000-201066	July 18, 2000	Japan			Abstract	
↓	2001-500682	January 16, 2001	Japan			Abstract	
/T.T./	05-509184	December 16, 2003	Japan			English Equivalent = USP 5,193,202 cited above	

OTHER DOCUMENTS

EXAMINER'S INITIALS	AUTHOR, TITLE, DATE, PERTINENT PAGES, ETC.
/T.T./	Abnous et al., "Ultra-Low-Power Domain-Specific Multimedia Processors," U.C. Berkeley, 1996 IEEE, pp. 461-470.
/T.T./	Albahama, O.T. et al., "On the Viability of FPGA-Based Integrated Coprocessors," Dept. of Electrical and Electronic Engineering, Imperial College of Science, London, 1999 IEEE, pp. 206-215.
/T.T./	Altera, "Flex 8000 Programmable Logic Device Family," Altera Corporation product description, January 2003, pp. 1-62.

INFORMATION DISCLOSURE STATEMENT BY APPLICANTS PTO-1449

Attorney Docket No.
2885/93

Serial No.
10/523,764

Applicant(s)
Vorbach et al.

Filing Date
August 2, 2005

Group Art Unit
2187

EXAMINER'S INITIALS	AUTHOR, TITLE, DATE, PERTINENT PAGES, ETC.
/T.T./	Altera, "Flex 10K Embedded Programmable Logic Device Family," Altera Corporation product description, January 2003, pp. 1-128.
	Athanas et al., "Processor Reconfiguration Through Instruction-Set Metamorphosis," 1993, IEEE Computers, pp. 11-18.
	Atmel, 5-K-50K Gates Coprocessor FPGA with Free Ram, Data Sheet, July 2006, 55 pages.
	Atmel, FPGA-based FIR Filter Application Note, September 1999, 10 pages.
	Atmel, "An Introduction to DSP Applications using the AT40K FPGA," FPGA Application Engineering, San Jose, CA, April 2004, 15 pages.
	Atmel, Configurable Logic Design & Application Book, Atmel Corporation, 1995, pp. 2-19 through 2-25.
	Atmel, Field Programmable Gate Array Configuration Guide, AT6000 Series Configuration Data Sheet, September 1999, pp. 1-20.
	Bacon, D. et al., "Compiler Transformations for High-Performance Computing," ACM Computing Surveys, 26(4):325-420 (1994)
	Bakkes, P.J., et al., "Mixing Fixed and Reconfigurable Logic for Array Processing," Dept. of Electrical and Electronic Engineering, University of Stellenbosch, South Africa, 1996 IEEE, pp. 118-125.
	Beck et al., "From control flow to data flow," TR 89-1050, October 1989, Dept. of Computer Science, Cornell University, Ithaca, NY, pp. 1-25.
	Becker, J. et al., "Architecture, Memory and Interface Technology Integration of an Industrial/Academic Configurable System-on-Chip (CSoC)," IEEE Computer Society Annual Workshop on VLSI (WVLSI 2003), (February 2003)
	Becker, J., "Configurable Systems-on-Chip (CSoC)," (Invited Tutorial), Proc. of 9th Proc. of XV Brazilian Symposium on Integrated Circuit, Design (SBCCI 2002), (September 2002)
	Becker et al., "Automatic Parallelism Exploitation for FPL-Based Accelerators," 1998, Proc. 31 st Annual Hawaii International Conference on System Sciences, pp. 169-178.
	Bratt, A., "Motorola field programmable analogue arrays, present hardware and future trends," Motorola Programmable Technology Centre, Gadbrook Business Centre, Northwich, Cheshire, 1998, The Institute of Electrical Engineers, IEE, Savoy Place, London, pp. 1-5.
	Cardoso, J.M.P. et al., "A novel algorithm combining temporal partitioning and sharing of functional units," University of Algarve, Faro, Portugal, 2001 IEEE, pp. 1-10.
	Cardoso, Joao M.P. and Markus Weinhardt, "XPP-VC: A C Compiler with Temporal Partitioning for the PACT-XPP Architecture," Field-Programmable Logic and Applications. Reconfigurable Computing is Going Mainstream, 12 th International Conference FPL 2002, Proceedings (Lecture Notes in Computer Science, Vol. 2438) Springer-Verlag Berlin, Germany, 2002, pp. 864-874.
	Cardoso, J.M.P. et al., "Compilation and Temporal Partitioning for a Coarse-Grain Reconfigurable Architecture," LYSACHT, P. & ROSENTIEL, W. eds., "New Algorithms, Architectures and Applications for Reconfigurable Computing," (2005) pp. 105-115
	Cardoso, J.M.P. et al., "Macro-Based Hardware Compilation of Java™ Bytecodes into a Dynamic Reconfigurable Computing System," Field-Programmable Custom Computing Machines (1999) FCCM '99. Proceedings. Seventh Annual IEEE Symposium on NAPA Valley, CA, USA, 21-23 April 1999, IEEE Comput. Soc, US, (21 April 1999) pp.2-11
	Clearspeed, CSX Processor Architecture, Whitepaper, PN-1110-0702, 2007, pp. 1-15, www.clearspeed.com .
	Clearspeed, CSX Processor Architecture, Whitepaper, PN-1110-0306, 2006, pp. 1-14, www.clearspeed.com .
	Compton, K. et al., "Configurable Computing: A Survey of Systems and Software," Northwestern University, Dept. of ECE, Technical Report, 1999, (XP-002315148), 39 pages.
	Cook, Jeffrey J., "The Amalgam Compiler Infrastructure," Thesis at the University of Illinois at Urbana-Champaign (2004) Chapter 7 & Appendix G
	Cronquist, D. et al., "Architecture Design of Reconfigurable Pipelined Datapaths," Department of Computer Science and Engineering, University of Washington, Seattle, WA, Proceedings of the 20 th Anniversary Conference on Advanced Research in VLSI, 1999, pp. 1-15.
	DeHon, A., "DPGA Utilization and Application," MIT Artificial Intelligence Laboratory, Proceedings of the Fourth International ACM Symposium on Field-Programmable Gate Arrays (FPGA '96), IEEE Computer Society, pp. 1-7.
/T.T./	DeHon, Andre, "Reconfigurable Architectures for General-Purpose Computing," Massachusetts Institute of Technology, Technical Report AITR-1586, October 1996 (1996-10), XP002445054, Cambridge, MA, pp. 1-353.

INFORMATION DISCLOSURE STATEMENT BY APPLICANTS PTO-1449	Attorney Docket No. 2885/93	Serial No. 10/523,764
	Applicant(s) Vorbach et al.	
	Filing Date August 2, 2005	Group Art Unit 2187

EXAMINER'S INITIALS	AUTHOR, TITLE, DATE, PERTINENT PAGES, ETC.
/T.T./	Diniz, P., et al., "A behavioral synthesis estimation interface for configurable computing," University of Southern California, Marina Del Rey, CA, 2001 IEEE, pp. 1-2.
	Ebeling, C. et al., "Mapping Applications to the RaPiD Configurable Architecture," Department of Computer Science and Engineering, University of Washington, Seattle, WA, FPGAs for Custom Computing Machines, 1997. <u>Proceedings, The 5th Annual IEEE Symposium</u> , Publication Date: 16-18 Apr 1997, 10 pages.
	Equator, Pixels to Packets, Enabling Multi-Format High Definition Video, Equator Technologies BSP-15 Product Brief, www.equator.com , 2001, 4 pages.
	Fawcett, B.K., "Map, Place and Route: The Key to High-Density PLD Implementation," Wescon Conference, IEEE Center (7 November 1995) pp. 292-297
	Franklin, Manoj et al., "A Fill-Unit Approach to Multiple Instruction Issue," Proceedings of the Annual International Symposium on Microarchitecture, November 1994, pp. 162-171.
	Freescall Slide Presentation, An Introduction to Motorola's RCF (Reconfigurable Compute Fabric) Technology, Presented by Frank David, Launched by Freescall Semiconductor, Inc., 2004, 39 pages.
	Genius, D. et al., "A Case for Array Merging in Memory Hierarchies," Proceedings of the 9th International Workshop on Compilers for Parallel Computers, CPC'01 (June 2001), 10 pages.
	Hartenstein, R. et al., "A new FPGA architecture for word-oriented datapaths," Proc. FPL'94, Springer LNCS, September 1994, pp. 144-155.
	Hartenstein, R., "Coarse grain reconfigurable architectures," Design Automation Conference, 2001, Proceedings of the ASP-DAC 2001 Asia and South Pacific, January 30- February 2, 2001, IEEE 30 January 2001, pp. 564-569.
	Hendrich, N., et al., "Silicon Compilation and Rapid Prototyping of Microprogrammed VLSI-Circuits with MIMOLA and SOLO 1400," Microprocessing & Microprogramming (September 1992) vol.35(1-5), pp. 287-294
	Hwang, K., "Advanced Computer Architecture - Parallelism, Scalability, Programmability," 1993, McGraw-Hill, Inc., pp. 348-355.
	Hwang, K., "Computer Architecture and Parallel Processing," Data Flow Computers and VLSI Computations, XP-002418655, 1985 McGraw-Hill, Chapter 10, pp. 732-807.
	IBM Technical Disclosure Bulletin, IBM Corp., New York, XP000424878, Bd. 36, Nr. 11, 1 November 1993, pp. 335-336.
	Inside DSP, "Ambric Discloses Massively Parallel Architecture," August 23, 2006, HTTP://insidedsp.com/tabid/64/articleType/ArticleView/articleId/155/Default.aspx , 2 pages.
	Intel, Intel MXP5800/MXP5400 Digital Media Processors, Architecture Overview, June 2004, Revision 2.4, pp. 1-24.
	Kaul, M., et al., "An automated temporal partitioning and loop fission approach of FPGA based reconfigurable synthesis of DSP applications," University of Cincinnati, Cincinnati, OH, ACM 1999, pp. 616-622.
	Kean, T.A., "Configurable Logic: A Dynamically Programmable Cellular Architecture and its VLSI Implementation," University of Edinburgh (Dissertation) 1988, pp. 1-286
	Kean, T., et al., "A Fast Constant Coefficient Multiplier for the XC6200," Xilinx, Inc., Lecture Notes in Computer Science, Vol. 1142, Proceedings of the 6th International Workshop of Field-Programmable Logic, 1996, 7 pages.
	Kim et al., "A Reconfigurable Multifunction Computing Cache Architecture," IEEE Transactions on Very Large Scale Integration (VLSI) Systems Volume 9, Issue 4, Aug 2001 Page(s):509 - 523.
	Knittel, Gunter, "A PCI-compatible FPGA-Coprocessor for 2D/3D Image Processing," University of Turgingen, Germany, 1996 IEEE, pp. 136-145.
	Koch, Andreas et al., "High-Level-Language Compilation for Reconfigurable Computers," Proceedings of European Workshop on Reconfigurable Communication-Centric SOCS (June 2005) 8 pages
	Koren et al., "A data-driven VLSI array for arbitrary algorithms," IEEE Computer Society, Long Beach, CA Vol. 21, No. 10, 1 October 1988, pp. 30-34.
	Larsen, S. et al., "Increasing and Detecting Memory Address Congruence," Proceedings of the 2002 IEEE International Conference on Parallel Architectures and Compilation Techniques (PACT'02), pp. 1-12 (September 2002).
	Lee et al., "A new distribution network based on controlled switching elements and its applications," IEEE/ACT Trans. of Networking, Vol. 3, No. 1, pp. 70-81, February 1995.
/T.T./	Lee, Jong-eun et al., "Reconfigurable ALU Array Architecture with Conditional Execution," International Soc. Design Conference (ISOOC) [online] October 25, 2004, Seoul, Korea, 5 pages.

INFORMATION DISCLOSURE STATEMENT BY APPLICANTS PTO-1449	Attorney Docket No. 2885/93	Serial No. 10/523,764
	Applicant(s) Vorbach et al.	
	Filing Date August 2, 2005	Group Art Unit 2187

EXAMINER'S INITIALS	AUTHOR, TITLE, DATE, PERTINENT PAGES, ETC.
/T.T./	Ling, X., "WASMII: An MPLD with Data-Driven Control on a Virtual Hardware," Journal of Supercomputing, Kluwer Academic Publishers, Dordrecht, Netherlands, 1995, pp. 253-276.
	Ling et al., "WASMII: A Multifunction Programmable Logic Device (MPLD) with Data Driven Control," The Transactions of the Institute of Electronics, Information and Communication Engineers, 25 April 1994, Vol. J77-D-1, Nr. 4, pp. 309-317. [This references is in Chinese, but should be comparable in content to the Ling et al. reference above]
	Margolus, N., "An FPGA architecture for DRAM-based systolic computations," Boston University Center for Computational Science and MIT Artificial Intelligence Laboratory, IEEE 1997, pp. 2-11.
	Mei, Bingfeng, "A Coarse-Grained Reconfigurable Architecture Template and Its Compilation Techniques," Katholieke Universiteit Leuven, PhD Thesis, January 2005, IMEC vzw, Universitair Micro-Electronica Centrum, Belgium, pp. 1-195 (and Table of Contents).
	Mei, Bingfeng, et al., "Design and Optimization of Dynamically Reconfigurable Embedded Systems," IMEC vzw, 2003, Belgium, 7 pages, http://www.imec.be/reconfigurable/pdf/ICERSA_01_design.pdf .
	Miyamori, T. et al., "REMARC: Reconfigurable Multimedia Array Coprocessor," Computer Systems Laboratory, Stanford University, IEICE TRANSACTIONS ON INFORMATION AND SYSTEMS E SERIES D, 1999; (abstract): Proceedings of the 1998 ACM/SIGDA sixth international symposium on Field programmable gate arrays, p.261, February 22-25, 1998, Monterey, California, United States, pp. 1-12.
	Moraes, F., et al., "A Physical Synthesis Design Flow Based on Virtual Components," XV Conference on Design of Circuits and Integrated Systems (November 2000) 6 pages
	Muchnick, S., "Advanced Compiler Design and Implementation" (Morgan Kaufmann 1997), Table of Contents, 11 pages
	Murphy, C., "Virtual Hardware Using Dynamic Reconfigurable Field Programmable Gate Arrays," Engineering Development Centre, Liverpool John Moores University, UK, GERI Annual Research Symposium 2005, 8 pages.
	Nageldinger, U., "Design-Space Exploration for Coarse Grained Reconfigurable Architectures," (Dissertation) Universitaet Kaiserslautern, 2000, Chapter 2, pp. 19-45.
	Neumann, T., et al., "A Generic Library for Adaptive Computing Environments," Field Programmable Logic and Applications, 11 th International Conference, FPL 2001, Proceedings (Lecture Notes in Computer Science, vol. 2147) (2001) pp. 503-512
	Olukotun, K., "The Case for a Single-Chip Microprocessor," ACM Sigplan Notices, ACM, Association for Computing Machinery, New York, Vol. 31, No. 9, September 1996 (1996-09-00) pp. 2-11.
	Ozawa, Motokazu et al., "A Cascade ALU Architecture for Asynchronous Super-Scalar Processors," IEICE Transactions on Electronics, Electronics Society, Tokyo, Japan, Vol. E84-C, No. 2, February 2001, pp. 229-237.
	PACT Corporation, "The XPP Communication System," Technical Report 15 (2000), pp. 1-16.
	Quenot, G.M., et al., "A Reconfigurable Compute Engine for Real-Time Vision Automata Prototyping," Laboratoire Systeme de Perception, DGA/Etablissement Technique Central de l'Armement, France, 1994 IEEE, pp. 91-100.
	Parhami, B., "Parallel Counters for Signed Binary Signals," Signals, Systems and Computers, 1989, Twenty-Third Asilomar Conference, Volume 1, pp. 513-516.
	Saleeba, Z.M.G., "A Self-Reconfiguring Computer System," Department of Computer Science, Monash University (Dissertation) 1998, pp. 1-306.
	Schmidt, H. et al., "Behavioral synthesis for FPGA-based computing," Carnegie Mellon University, Pittsburgh, PA, 1994 IEEE, pp. 125-132.
	Schönfeld, M., et al., "The LISA Design Environment for the Synthesis of Array Processors Including Memories for the Data Transfer and Fault Tolerance by Reconfiguration and Coding Techniques," J. VLSI Signal Processing Systems for Signal, Image, and Video Technology, (1 October 1995) vol. 11(1/2), pp. 51-74
	Shin, D., et al., "C-based Interactive RTL Design Methodology," Technical Report CECS-03-42 (December 2003) pp. 1-16
	Singh, H. et al., "MorphoSys: An Integrated Reconfigurable System for Data-Parallel Computation-Intensive Applications," University of California, Irvine, CA. and Federal University of Rio de Janeiro, Brazil, 2000, IEEE Transactions on Computers, pp. 1-35.
	Sondervan, J., "Retiming and logic synthesis," Electronic Engineering (January 1993) vol. 65(793), pp.33, 35-36
/T.T./	Soni, M., "VLSI Implementation of a Wormhole Run-time Reconfigurable Processor," June 2001, (Masters Thesis) Virginia Polytechnic Institute and State University, 88 pages.

INFORMATION DISCLOSURE STATEMENT BY APPLICANTS PTO-1449	Attorney Docket No. 2885/93	Serial No. 10/523,764
	Applicant(s) Vorbach et al.	
	Filing Date August 2, 2005	Group Art Unit 2187

EXAMINER'S INITIALS	AUTHOR, TITLE, DATE, PERTINENT PAGES, ETC.
/T.T./	Sueyoshi, T, "Present Status and Problems of the Reconfigurable Computing Systems Toward the Computer Evolution," Department of Artificial Intelligence, Kyushu Institute of Technology, Fukuoka, Japan; Institute of Electronics, Information and Communication Engineers, Vol. 96, No. 426, IEICE Technical Report (1996), pp. 111-119 [English Abstract Only]
	Sutton et al., "A Multiprocessor DSP System Using PADDI-2," U.C. Berkeley, 1998 ACM, pp. 62-65.
	Tsutsui, A., et al., "YARDS: FPGA/MPU Hybrid Architecture for Telecommunication Data Processing," NTT Optical Network Systems Laboratories, Japan, 1997 ACM, pp. 93-99.
	Vasell et al., "The Function Processor: A Data-Driven Processor Array for Irregular Computations," Chalmers University of Technology, Sweden, pp. 1-21
	Waingold, E., et al., "Baring it all to software: Raw machines," IEEE Computer, September 1997, at 86-93
	Weinhardt, M., "Compilation Methods for Structure-programmable Computers," dissertation, ISBN 3-89722-011-3, 1997. [TABLE OF CONTENTS AND ENGLISH ABSTRACT PROVIDED]
	Weinhardt, Markus et al., "Pipeline Vectorization," IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, Vol. 20, No. 2, February 2001, pp. 234-248.
	Weinhardt, Markus et al., "Memory Access Optimization for Reconfigurable Systems," IEEE Proceedings Computers and Digital Techniques, 48(3) (May 2001) pp. 1-16.
	Wolfe, M. et al., "High Performance Compilers for Parallel Computing" (Addison-Wesley 1996) Table of Contents, 11 pages.
	XILINX, "Spartan and SpartanXL Families Field Programmable Gate Arrays," January 1999, Xilinx, pp. 4-3 through 4-70.
	XILINX, "XC6200 Field Programmable Gate Arrays," April 24, 1997, Xilinx product description, pp. 1-73.
	XILINX, "XC3000 Series Field Programmable Gate Arrays," November 6, 1998, Xilinx product description, pp. 1-76.
	XILINX, "XC4000E and XC4000X Series Field Programmable Gate Arrays," May 14, 1999, Xilinx product description, pp. 1-68.
	XILINX, "Virtex-E 1.8 V Extended Memory Field Programmable Gate Arrays," July 17, 2002, Xilinx Production Product Specification, pp. 1-118.
	XILINX, "Virtex-II and Virtex-II Pro X FPGA User Guide," March 28, 2007, Xilinx user guide, pp. 1-559.
	Zhang, et al., "A 1-V Heterogeneous Reconfigurable DSP IC for Wireless Baseband Digital Signal Processing," IEEE Journal of Solid-State Circuits, Vol. 35, No. 11, November 2000, pp. 1697-1704.
↓	Zhang et al., "Abstract: Low-Power Heterogeneous Reconfigurable Digital Signal Processors with Energy-Efficient Interconnect Network," U.C. Berkeley (2004), pp. 1-120.
/T.T./	Zima, H. et al., "Supercompilers for parallel and vector computers" (Addison-Wesley 1991) Table of Contents, 5 pages.

EXAMINER	/Tuan Thai/	DATE CONSIDERED	02/12/2010
EXAMINER: Initial if citation considered, whether or not citation is in conformance with M.P.E.P. 609; draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.			



2185

U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE			
SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT		Docket Number: 2885/93	
Application Number 10/523,764	Filing Date August 2, 2005	Examiner Tuan V. Thai	Art Unit 2185
Invention Title DATA PROCESSING DEVICE AND METHOD		Inventor(s) Martin Vorbach et al.	

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to:
Mail Stop: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on
Date: March 13, 2009
Signature: [Signature]
Michelle M. Carniaux, Reg. No. 36,098

Sir:

Pursuant to 37 CFR § 1.56, the attention of the Patent and Trademark Office is hereby directed to the reference(s) listed on the attached PTO-1449. It is respectfully requested that the information be expressly considered during the prosecution of this application, and that the reference(s) be made of record therein and appear among the "References Cited" on any patent to issue therefrom. The filing of this Information Disclosure Statement and the enclosed PTO Form No. 1449, shall not be construed as an admission that the information cited is prior art, or is considered to be material to patentability as defined in 37 C.F.R. § 1.56(b). The paragraphs marked below are applicable. It is believed that no fees other than those indicated below are due, but authorization is hereby given to charge any additional fees due, or to credit any overpayment, to Kenyon & Kenyon LLP, deposit account 11-0600.

☐ 1. This Information Disclosure Statement is being filed (a) within three months of the filing date of a national application other than a continued prosecution application under 37 C.F.R. § 1.53(d), (b) within three months of the date of entry of the national stage as set forth in 37 C.F.R. § 1.491 in an international application, (c) before the mailing date of a first Office Action on the merits in the present application, OR (d) before the mailing of a first office action after filing of a request for continued examination. No certification or fee is required.

☒ 2. This Information Disclosure Statement is being filed more than three months after the U.S. filing date AND after the mailing date of the first Office Action on the merits, but before the mailing date of a final action, Notice of Allowance, or any action that otherwise closes prosecution.

☐ a. I hereby certify that each item of information contained in this Information Disclosure Statement was first cited in a communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of this Information Disclosure Statement. 37 CFR § 1.97(e)(1).

☐ b. I hereby certify that no item of information in this Information Disclosure Statement was cited in a communication from a foreign patent office in a counterpart foreign application or, to my knowledge after making reasonable inquiry,


was known to any individual designated in 37 CFR §1.56(c) more than three months prior to the filing of this Information Disclosure Statement. 37 CFR §1.97(e)(2).

☒ c. Please debit **Kenyon & Kenyon LLP, Deposit Account No. 11-0600** in the amount of \$180.00 in payment of the fee under 37 CFR §1.17(p) to ensure consideration of the disclosed information.

☒ 3. Since this application was filed after June 30, 2003, copies of U.S. references are not included.

Respectfully submitted,

Date: 13 March 2009


Michelle M. Carniaux
Reg. No. 36,098

KENYON & KENYON LLP
One Broadway
New York, NY 20004
(212) 425-7200 telephone
(212) 425-5288 facsimile
CUSTOMER NUMBER 26646

Transaction List

Search by

☐ Accounting Date: Operator ID:
(MMDDYY)



☒ Name/Number: Starts: Ends:
☐ Attny Docket No.:
☐ Deposit Account No.:

Accounting Date	Operator ID	Seq. No.	Txn Src	Fee Code	St	Amount	Name/Number
03/17/2009	INTEFSW	1469	SALE	1806	A	180.00	10523764
10/31/2008	INTEFSW	19935	SALE	2255	A	1,175.00	10523764
12/28/2007	INTEFSW	12453	SALE	2253	A	525.00	10523764
12/28/2007	INTEFSW	12452	SALE	2616	A	185.00	10523764
12/28/2007	INTEFSW	12451	SALE	2614	A	420.00	10523764
12/28/2007	INTEFSW	12450	SALE	2615	A	7,000.00	10523764
08/28/2007	WABDELR1	294	SALE	1806	A	180.00	10523764
08/09/2005	ATRAN1	8	SALE	2617	A	65.00	10523764
08/08/2005	ECOOPER	26	SALE	8021	A	40.00	10523764
07/13/2005	KBALTIMO	3	SALE	2681	A	250.00	10523764
07/13/2005	KRALTIMO	2	SALE	2642	A	200.00	10523764

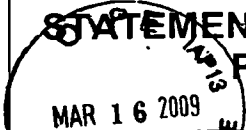
<



Adjustment Detail

Authorization Detail



INFORMATION DISCLOSURE STATEMENT BY APPLICANTS PTO-1449 	Attorney Docket No. 2885/93	Serial No. 10/523,764
	Applicant(s) Vorbach et al.	
	Filing Date August 2, 2005	Group Art Unit 2187

U.S. PATENT DOCUMENTS

EXAMINER'S INITIALS	PATENT/ PUBLICATION NUMBER	PATENT/PUBLICATION DATE	NAME	CLASS	SUBCLASS	FILING DATE
	RE34,444	November 1993	Kaplinsky			
	RE37,195	May 29, 2001	Kean			
	4,414,547	November 1983	Knapp et al.			
	4,590,583	May 20, 1986	Miller			
	4,667,190	May 1987	Fant et al.			
	4,882,687	November 1989	Gordon			
	4,884,231	November 1980	Mor et al.			
	4,918,440	April 17, 1990	Furtek et al.			
	4,972,314	November 1990	Getzinger et al.			
	5,010,401	April 1991	Murakami et al.			
	5,034,914	July 1991	Osterlund			
	5,041,924	August 1991	Blackborow et al.			
	5,099,447	March 1992	Myszewski			
	5,193,202	March 1993	Jackson et al.			
	5,212,716	May 1993	Ferraiolo et al.			
	5,218,302	June 8, 1993	Loewe et al.			
	5,237,686	August 1993	Asano et al.			
	5,276,836	January 4, 1994	Fukumaru et al.			
	5,327,125	July 1994	Iwase et al.			
	5,343,406	Aug 30, 1994	Freeman et al.			
	5,418,953	May 1995	Hunt et al.			
	5,469,003	November 1995	Kean			
	5,537,580	July 1996	Giomi et al.			
	5,550,782	Aug 27, 1996	Cliff et al.			
	5,581,731	December 3, 1996	King et al.			
	5,625,836	Apr 29, 1997	Barker et al.			
	5,646,544	Jul 8, 1997	Iadanza			
	5,646,545	Jul 8, 1997	Trimberger et al.			
	5,652,529	July 1997	Gould et al.			
	5,737,565	April 1998	Mayfield			
	5,748,979	May 1998	Trimberger			
	5,752,035	May 1998	Trimberger			
	5,754,459	May 19, 1998	Telikepalli			
	5,754,820	May 19, 1998	Yamagami			
	5,781,756	Jul 14, 1998	Hung			
	5,781,756	Jul 14, 1998	Hung			
	5,801,547	September 1, 1998	Kean			
	5,801,958	September 1998	Dangelo et al.			

INFORMATION DISCLOSURE STATEMENT BY APPLICANTS PTO-1449	Attorney Docket No. 2885/93	Serial No. 10/523,764
	Applicant(s) Vorbach et al.	
	Filing Date August 2, 2005	Group Art Unit 2187

EXAMINER'S INITIALS	PATENT/ PUBLICATION NUMBER	PATENT/PUBLICATION DATE	NAME	CLASS	SUBCLASS	FILING DATE
	5,815,715	September 1998	Kayhan			
	5,821,774	October 1998	Veytsman et al.			
	5,831,448	Nov 3, 1998	Kean			
	5,844,422	December 1, 1998	Trimberger et al.			
	5,857,097	January 1999	Henzinger et al.			
	5,862,403	January 1999	Kanai et al.			
	5,870,620	Feb 9, 1999	Kadosumi et al.			
	5,889,533	Mar 30, 1999	Lee			
	5,933,023	Aug 3, 1999	Young			
	5,960,193	September 28, 1999	Guttag et al.			
	5,966,143	Oct 12, 1999	Breternitz, Jr.			
	5,978,583	November 1999	Ekanadham et al.			
	5,999,990	December 1999	Sharrit et al.			
	6,020,760	February 1, 2000	Sample et al.			
	6,026,481	February 2000	New et al.			
	6,044,030	Mar 28, 2000	Zheng et al.			
	6,077,315	June 2000	Greenbaum et a.			
	6,084,429	July 2000	Trimberger			
	6,105,106	August 2000	Manning			
	6,134,166	October 17, 2000	Lytle et al.			
	6,137,307	October 2000	Iwanczuk et al.			
	6,154,048	November 2000	Iwanczuk et al.			
	6,154,049	Nov 28, 2000	New			
	6,157,214	December 5, 2000	Marshall			
	6,185,256	February 2001	Saito et al.			
	6,185,731	February 2001	Maeda et al.			
	6,188,240	February 2001	Nakaya			
	6,198,304	March 2001	Sasaki			
	6,201,406	March 2001	Iwanczuk et al.			
	6,204,687	March 2001	Schultz et al.			
	6,215,326	April 10, 2001	Jefferson et al.			
	6,216,223	April 2001	Revilla et al.			
	6,252,792	June 26, 2001	Marshall et al.			
	6,256,724	July 2001	Hocevar et al.			
	6,262,908	July 17, 2001	Marshall et al.			
	6,266,760	July 2001	DeHon et al.			
	6,285,624	September 2001	Chen			
	6,311,265	October 2001	Beckerle et al.			
	6,353,841	March 5, 2002	Marshall et al.			

INFORMATION DISCLOSURE STATEMENT BY APPLICANTS PTO-1449	Attorney Docket No. 2885/93	Serial No. 10/523,764
	Applicant(s) Vorbach et al.	
	Filing Date August 2, 2005	Group Art Unit 2187

EXAMINER'S INITIALS	PATENT/ PUBLICATION NUMBER	PATENT/PUBLICATION DATE	NAME	CLASS	SUBCLASS	FILING DATE
	6,362,650	Mar 26, 2002	New et al.			
	6,374,286	April 2002	Gee			
	6,373,779	Apr 16, 2002	Pang et al.			
	6,381,624	April 2002	Colon-Bonet et al.			
	6,400,601	June 2002	Sudo et al.			
	6,421,808	July 2002	McGeer			
	6,421,809	July 2002	Wuytack et al.			
	6,425,054	July 23, 2002	Nguyen			
	6,427,156	Jul 30, 2002	Chapman et al.			
	6,430,309	August 2002	Pressman et al.			
	6,434,642	Aug 13, 2002	Camilleri et al.			
	6,434,699	August 13, 2002	Jones et al.			
	6,435,054	October 10,2000	Nguyen			
	6,438,747	August 2002	Schreiber et al.			
	6,476,634	November 2002	Bilski			
	6,487,709	November 2002	Keller et al.			
	6,490,695	December 2002	Zagorski et al.			
	6,507,947	January 2003	Schreiber et al.			
	6,516,382	February 2003	Manning			
	6,518,787	February 2003	Allegrucci et al.			
	6,523,107	February 18, 2003	Stansfield et al.			
	6,525,678	February 2003	Veenstra et al.			
	6,539,415	March 25, 2003	Mercs			
	6,539,438	March 25, 2003	Ledzius et al.			
	6,542,394	April 1, 2003	Marshall et al.			
	6,542,844	April 2003	Hanna			
	6,553,395	April 22, 2003	Marshall et al.			
	6,567,834	May 20, 2003	Marshall et al.			
	6,631,487	October 2003	Abramovici et al.			
	6,633,181	October 2003	Rupp			
	6,658,564	December 2003	Smith et al.			
	6,708,325	March 2004	Cooke et al.			
	6,754,805	June 2004	Yujen Juan			
	6,757,847	June 2004	Farkash et al.			
	6,757,892	June 2004	Gokhale et al.			

INFORMATION DISCLOSURE STATEMENT BY APPLICANTS PTO-1449	Attorney Docket No. 2885/93	Serial No. 10/523,764
	Applicant(s) Vorbach et al.	
	Filing Date August 2, 2005	Group Art Unit 2187

EXAMINER'S INITIALS	PATENT/ PUBLICATION NUMBER	PATENT/PUBLICATION DATE	NAME	CLASS	SUBCLASS	FILING DATE
	6,782,445	August 2004	Olgiati et al.			
	6,785,826	August 31, 2004	Durham et al.			
	6,802,206	October 2004	Patterson et al.			
	6,803,787	October 2004	Wicker, Jr.			
	6,820,188	November 16, 2004	Stansfield et al.			
	6,829,697	December 2004	Davis et al.			
	6,847,370	January 2005	Baldwin et al.			
	6,871,341	March 2005	Shyr			
	6,874,108	March 2005	Abramovici et al.			
	6,886,092	April 2005	Douglass et al.			
	6,901,502	May 2005	Yano et al.			
	6,961,924	November 2005	Bates et al.			
	6,928,523	August 2005	Yamada, Akira			
	6,977,649	December 2005	Baldwin et al.			
	7,000,161	February 2006	Allen et al.			
	7,007,096	February 2006	Lisitsa et al.			
	7,010,687	March 2006	Ichimura			
	7,038,952	May 2, 2006	Zack et al.			
	7,210,129	April 2007	May et al.			
	7,237,087	June 26, 2007	Vorbach et al.			
	7,249,351	July 2007	Songer et al.			
	7,254,649	August 2007	Subramanian et al.			
	7,340,596	March 2008	Crosland et al.			
	7,350,178	March 2008	Crosland et al.			
	2001/001860	May 2001	Bieu			
	2001/010074	July 26, 2001	Nishihara et al.			
	2001/032305	October 2001	Barry			
	2002/083308	June 27, 2002	Pereira et al.			
	2002/103839	August 2002	Ozawa			
	2002/124238	September 05, 2002	Metzgen			
	2002/138716	September 26, 2002	Master et al.			
	2003/001615	January 2003	Sueyoshi et al.			
	2003/061542	March 2003	Bates et al.			
	2003/062922	Apr 3, 2003	Douglass et al.			
	2003/086300	May 2003	Noyes et al.			

INFORMATION DISCLOSURE STATEMENT BY APPLICANTS PTO-1449	Attorney Docket No. 2885/93	Serial No. 10/523,764
	Applicant(s) Vorbach et al.	
	Filing Date August 2, 2005	Group Art Unit 2187

EXAMINER'S INITIALS	PATENT/ PUBLICATION NUMBER	PATENT/PUBLICATION DATE	NAME	CLASS	SUBCLASS	FILING DATE
	2005/066213	March 2005	Vorbach et al.			
	2005/0144210	Jun 30, 2005	Simkins et al.			
	2005/0144212	Jun 30, 2005	Simkins et al.			
	2005/0144215	Jun 30, 2005	Simkins et al.			
	2006/0130096	Oct 12, 2006	Thendean et al.			
	2006/0230094	Oct 12, 2006	Simkins et al.			

FOREIGN PATENT DOCUMENTS

EXAMINER'S INITIALS	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATION	
						YES	NO
	0 398 552	November 22, 1990	EPO				
	0 746 106	December 4, 1996	EPO				
	1 061 439	December 20, 2000	EPO				
	1 669 885	Jun 14, 2006	EPO			Abstract	
	WO92/001987	February 6, 1992	PCT				
	WO98/010517	March 12, 1998	PCT				
	WO98/035294	August 13, 1998	PCT				
	WO00/049496	August 24, 2000	PCT				
	WO00/077652	December 21, 2000	PCT				
	WO02/050665	June 27, 2002	PCT				
	WO02/071196	September 12, 2002	PCT				
	WO04/114128	December 29, 2004	PCT				
	WO04/053718	June 24, 2004	PCT				
	WO05/045692	May 19, 2005	PCT				
	08069447	March 12, 1996	Japan			Abstract	
	2000-201066	July 18, 2000	Japan			Abstract	
	2001-500682	January 16, 2001	Japan			Abstract	
	05-509184	December 16, 2003	Japan			English Equivalent = USP 5,193,202 cited above	

OTHER DOCUMENTS

EXAMINER'S INITIALS	AUTHOR, TITLE, DATE, PERTINENT PAGES, ETC.
	Abnous et al., "Ultra-Low-Power Domain-Specific Multimedia Processors," U.C. Berkeley, 1996 IEEE, pp. 461-470.
	Albahama, O.T. et al., "On the Viability of FPGA-Based Integrated Coprocessors," Dept. of Electrical and Electronic Engineering, Imperial College of Science, London, 1999 IEEE, pp. 206-215.
	Altera, "Flex 8000 Programmable Logic Device Family," Altera Corporation product description, January 2003, pp. 1-62.

INFORMATION DISCLOSURE STATEMENT BY APPLICANTS PTO-1449	Attorney Docket No. 2885/93	Serial No. 10/523,764
	Applicant(s) Vorbach et al.	
	Filing Date August 2, 2005	Group Art Unit 2187

EXAMINER'S INITIALS	AUTHOR, TITLE, DATE, PERTINENT PAGES, ETC.
	Altera, "Flex 10K Embedded Programmable Logic Device Family," Altera Corporation product description, January 2003, pp. 1-128.
	Athanas et al., "Processor Reconfiguration Through Instruction-Set Metamorphosis," 1993, IEEE Computers, pp. 11-18.
	Atmel, 5-K-50K Gates Coprocessor FPGA with Free Ram, Data Sheet, July 2006, 55 pages.
	Atmel, FPGA-based FIR Filter Application Note, September 1999, 10 pages.
	Atmel, "An Introduction to DSP Applications using the AT40K FPGA," FPGA Application Engineering, San Jose, CA, April 2004, 15 pages.
	Atmel, Configurable Logic Design & Application Book, Atmel Corporation, 1995, pp. 2-19 through 2-25.
	Atmel, Field Programmable Gate Array Configuration Guide, AT6000 Series Configuration Data Sheet, September 1999, pp. 1-20.
	Bacon, D. et al., "Compiler Transformations for High-Performance Computing," ACM Computing Surveys, 26(4):325-420 (1994)
	Bakkes, P.J., et al., "Mixing Fixed and Reconfigurable Logic for Array Processing," Dept. of Electrical and Electronic Engineering, University of Stellenbosch, South Africa, 1996 IEEE, pp. 118-125.
	Beck et al., "From control flow to data flow," TR 89-1050, October 1989, Dept. of Computer Science, Cornell University, Ithaca, NY, pp. 1-25.
	Becker, J. et al., "Architecture, Memory and Interface Technology Integration of an Industrial/Academic Configurable System-on-Chip (CSoC)," IEEE Computer Society Annual Workshop on VLSI (WVLSI 2003), (February 2003)
	Becker, J., "Configurable Systems-on-Chip (CSoC)," (Invited Tutorial), Proc. of 9th Proc. of XV Brazilian Symposium on Integrated Circuit, Design (SBCCI 2002), (September 2002)
	Becker et al., "Automatic Parallelism Exploitation for FPL-Based Accelerators," 1998, Proc. 31 st Annual Hawaii International Conference on System Sciences, pp. 169-178.
	Bratt, A., "Motorola field programmable analogue arrays, present hardware and future trends," Motorola Programmable Technology Centre, Gadbrook Business Centre, Northwich, Cheshire, 1998, The Institute of Electrical Engineers, IEE, Savoy Place, London, pp. 1-5.
	Cardoso, J.M.P. et al., "A novel algorithm combining temporal partitioning and sharing of functional units," University of Algarve, Faro, Portugal, 2001 IEEE, pp. 1-10.
	Cardoso, Joao M.P. and Markus Weinhardt, "XPP-VC: A C Compiler with Temporal Partitioning for the PACT-XPP Architecture," Field-Programmable Logic and Applications. Reconfigurable Computing is Going Mainstream, 12 th International Conference FPL 2002, Proceedings (Lecture Notes in Computer Science, Vol. 2438) Springer-Verlag Berlin, Germany, 2002, pp. 864-874.
	Cardoso, J.M.P. et al., "Compilation and Temporal Partitioning for a Coarse-Grain Reconfigurable Architecture," LYSACHT, P. & ROSENTIEL, W. eds., "New Algorithms, Architectures and Applications for Reconfigurable Computing," (2005) pp. 105-115
	Cardoso, J.M.P. et al., "Macro-Based Hardware Compilation of Java™ Bytecodes into a Dynamic Reconfigurable Computing System," Field-Programmable Custom Computing Machines (1999) FCCM '99. Proceedings. Seventh Annual IEEE Symposium on NAPA Valley, CA, USA, 21-23 April 1999, IEEE Comput. Soc, US, (21 April 1999) pp.2-11
	Clearspeed, CSX Processor Architecture, Whitepaper, PN-1110-0702, 2007, pp. 1-15, www.clearspeed.com .
	Clearspeed, CSX Processor Architecture, Whitepaper, PN-1110-0306, 2006, pp. 1-14, www.clearspeed.com .
	Compton, K. et al., "Configurable Computing: A Survey of Systems and Software," Northwestern University, Dept. of ECE, Technical Report, 1999, (XP-002315148), 39 pages.
	Cook, Jeffrey J., "The Amalgam Compiler Infrastructure," Thesis at the University of Illinois at Urbana-Champaign (2004) Chapter 7 & Appendix G
	Cronquist, D. et al., "Architecture Design of Reconfigurable Pipelined Datapaths," Department of Computer Science and Engineering, University of Washington, Seattle, WA, Proceedings of the 20 th Anniversary Conference on Advanced Research in VLSI, 1999, pp. 1-15.
	DeHon, A., "DPGA Utilization and Application," MIT Artificial Intelligence Laboratory, Proceedings of the Fourth International ACM Symposium on Field-Programmable Gate Arrays (FPGA '96), IEEE Computer Society, pp. 1-7.
	DeHon, Andre, "Reconfigurable Architectures for General-Purpose Computing," Massachusetts Institute of Technology, Technical Report AITR-1586, October 1996 (1996-10), XP002445054, Cambridge, MA, pp. 1-353.

DUPLICATION

INFORMATION DISCLOSURE STATEMENT BY APPLICANTS PTO-1449	Attorney Docket No. 2885/93	Serial No. 10/523,764
	Applicant(s) Vorbach et al.	
	Filing Date August 2, 2005	Group Art Unit 2187

EXAMINER'S INITIALS	AUTHOR, TITLE, DATE, PERTINENT PAGES, ETC.
	Diniz, P., et al., "A behavioral synthesis estimation interface for configurable computing," University of Southern California, Marina Del Rey, CA, 2001 IEEE, pp. 1-2.
	Ebeling, C. et al., "Mapping Applications to the RaPiD Configurable Architecture," Department of Computer Science and Engineering, University of Washington, Seattle, WA, <u>FPGAs for Custom Computing Machines, 1997. Proceedings., The 5th Annual IEEE Symposium</u> , Publication Date: 16-18 Apr 1997, 10 pages.
	Equator, Pixels to Packets, Enabling Multi-Format High Definition Video, Equator Technologies BSP-15 Product Brief, www.equator.com , 2001, 4 pages.
	Fawcett, B.K., "Map, Place and Route: The Key to High-Density PLD Implementation," Wescon Conference, IEEE Center (7 November 1995) pp. 292-297
	Franklin, Manoj et al., "A Fill-Unit Approach to Multiple Instruction Issue," Proceedings of the Annual International Symposium on Microarchitecture, November 1994, pp. 162-171.
	Freescale Slide Presentation, An Introduction to Motorola's RCF (Reconfigurable Compute Fabric) Technology, Presented by Frank David, Launched by Freescale Semiconductor, Inc., 2004, 39 pages.
	Genius, D. et al., "A Case for Array Merging in Memory Hierarchies," Proceedings of the 9th International Workshop on Compilers for Parallel Computers, CPC'01 (June 2001), 10 pages.
	Hartenstein, R. et al., "A new FPGA architecture for word-oriented datapaths," Proc. FPL'94, Springer LNCS, September 1994, pp. 144-155.
	Hartenstein, R., "Coarse grain reconfigurable architectures," Design Automation Conference, 2001, Proceedings of the ASP-DAC 2001 Asia and South Pacific, January 30- February 2, 2001, IEEE 30 January 2001, pp. 564-569.
	Hendrich, N., et al., "Silicon Compilation and Rapid Prototyping of Microprogrammed VLSI-Circuits with MIMOLA and SOLO 1400," Microprocessing & Microprogramming (September 1992) vol.35(1-5), pp. 287-294
	Hwang, K., "Advanced Computer Architecture – Parallelism, Scalability, Programmability," 1993, McGraw-Hill, Inc., pp. 348-355.
	Hwang, K., "Computer Architecture and Parallel Processing," Data Flow Computers and VLSI Computations, XP-002418655, 1985 McGraw-Hill, Chapter 10, pp. 732-807.
	IBM Technical Disclosure Bulletin, IBM Corp., New York, XP000424878, Bd. 36, Nr. 11, 1 November 1993, pp. 335-336.
	Inside DSP, "Ambric Discloses Massively Parallel Architecture," August 23, 2006, HTTP://insidedsp.com/tabid/64/articleType/ArticleView/articleId/155/Default.aspx , 2 pages.
	Intel, Intel MXP5800/MXP5400 Digital Media Processors, Architecture Overview, June 2004, Revision 2.4, pp. 1-24.
	Kaul, M., et al., "An automated temporal partitioning and loop fission approach of FPGA based reconfigurable synthesis of DSP applications," University of Cincinnati, Cincinnati, OH, ACM 1999, pp. 616-622.
	Kean, T.A., "Configurable Logic: A Dynamically Programmable Cellular Architecture and its VLSI Implementation," University of Edinburgh (Dissertation) 1988, pp. 1-286
	Kean, T., et al., "A Fast Constant Coefficient Multiplier for the XC6200," Xilinx, Inc., Lecture Notes in Computer Science, Vol. 1142, Proceedings of the 6 th International Workshop of Field-Programmable Logic, 1996, 7 pages.
	Kim et al., "A Reconfigurable Multifunction Computing Cache Architecture," IEEE Transactions on Very Large Scale Integration (VLSI) Systems Volume 9, Issue 4, Aug 2001 Page(s):509 – 523.
	Knittel, Gunter, "A PCI-compatible FPGA-Coprocessor for 2D/3D Image Processing," University of Turgingen, Germany, 1996 IEEE, pp. 136-145.
	Koch, Andreas et al., "High-Level-Language Compilation for Reconfigurable Computers," Proceedings of European Workshop on Reconfigurable Communication-Centric SOCS (June 2005) 8 pages
	Koren et al., "A data-driven VLSI array for arbitrary algorithms," IEEE Computer Society, Long Beach, CA Vol. 21, No. 10, 1 October 1988, pp. 30-34.
	Larsen, S. et al., "Increasing and Detecting Memory Address Congruence," Proceedings of the 2002 IEEE International Conference on Parallel Architectures and Compilation Techniques (PACT'02), pp. 1-12 (September 2002).
	Lee et al., "A new distribution network based on controlled switching elements and its applications," IEEE/ACT Trans. of Networking, Vol. 3, No. 1, pp. 70-81, February 1995.
	Lee, Jong-eun et al., "Reconfigurable ALU Array Architecture with Conditional Execution," International Soc. Design Conference (ISOOC) [online] October 25, 2004, Seoul, Korea, 5 pages.

INFORMATION DISCLOSURE STATEMENT BY APPLICANTS PTO-1449	Attorney Docket No. 2885/93	Serial No. 10/523,764
	Applicant(s) Vorbach et al.	
	Filing Date August 2, 2005	Group Art Unit 2187

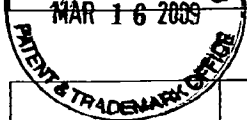
EXAMINER'S INITIALS	AUTHOR, TITLE, DATE, PERTINENT PAGES, ETC.
	Ling, X., "WASMII: An MPLD with Data-Driven Control on a Virtual Hardware," Journal of Supercomputing, Kluwer Academic Publishers, Dordrecht, Netherlands, 1995, pp. 253-276.
	Ling et al., "WASMII: A Multifunction Programmable Logic Device (MPLD) with Data Driven Control," The Transactions of the Institute of Electronics, Information and Communication Engineers, 25 April 1994, Vol. J77-D-1, Nr. 4, pp. 309-317. [This references is in Chinese, but should be comparable in content to the Ling et al. reference above]
	Margolus, N., "An FPGA architecture for DRAM-based systolic computations," Boston University Center for Computational Science and MIT Artificial Intelligence Laboratory, IEEE 1997, pp. 2-11.
	Mei, Bingfeng, "A Coarse-Grained Reconfigurable Architecture Template and Its Compilation Techniques," Katholieke Universiteit Leuven, PhD Thesis, January 2005, IMEC vzw, Universitair Micro-Electronica Centrum, Belgium, pp. 1-195 (and Table of Contents).
	Mei, Bingfeng, et al., "Design and Optimization of Dynamically Reconfigurable Embedded Systems," IMEC vzw, 2003, Belgium, 7 pages, http://www.imec.be/reconfigurable/pdf/ICERSA_01_design.pdf .
	Miyamori, T. et al., "REMARC: Reconfigurable Multimedia Array Coprocessor," Computer Systems Laboratory, Stanford University, IEICE TRANSACTIONS ON INFORMATION AND SYSTEMS E SERIES D, 1999; (abstract): Proceedings of the 1998 ACM/SIGDA sixth international symposium on Field programmable gate arrays, p.261, February 22-25, 1998, Monterey, California, United States, pp. 1-12.
	Moraes, F., et al., "A Physical Synthesis Design Flow Based on Virtual Components," XV Conference on Design of Circuits and Integrated Systems (November 2000) 6 pages
	Muchnick, S., "Advanced Compiler Design and Implementation" (Morgan Kaufmann 1997), Table of Contents, 11 pages
	Murphy, C., "Virtual Hardware Using Dynamic Reconfigurable Field Programmable Gate Arrays," Engineering Development Centre, Liverpool John Moores University, UK, GERI Annual Research Symposium 2005, 8 pages.
	Nageldinger, U., "Design-Space Exploration for Coarse Grained Reconfigurable Architectures," (Dissertation) Universitaet Kaiserslautern, 2000, Chapter 2, pp. 19-45.
	Neumann, T., et al., "A Generic Library for Adaptive Computing Environments," Field Programmable Logic and Applications, 11 th International Conference, FPL 2001, Proceedings (Lecture Notes in Computer Science, vol. 2147) (2001) pp. 503-512
	Olukotun, K., "The Case for a Single-Chip Microprocessor," ACM Sigplan Notices, ACM, Association for Computing Machinery, New York, Vol. 31, No. 9, September 1996 (1996-09-00) pp. 2-11.
	Ozawa, Motokazu et al., "A Cascade ALU Architecture for Asynchronous Super-Scalar Processors," IEICE Transactions on Electronics, Electronics Society, Tokyo, Japan, Vol. E84-C, No. 2, February 2001, pp. 229-237.
	PACT Corporation, "The XPP Communication System," Technical Report 15 (2000), pp. 1-16.
	Quenot, G.M., et al., "A Reconfigurable Compute Engine for Real-Time Vision Automata Prototyping," Laboratoire Systeme de Perception, DGA/Etablissement Technique Central de l'Armement, France, 1994 IEEE, pp. 91-100.
	Parhami, B., "Parallel Counters for Signed Binary Signals," Signals, Systems and Computers, 1989, Twenty-Third Asilomar Conference, Volume 1, pp. 513-516.
	Saleeba, Z.M.G., "A Self-Reconfiguring Computer System," Department of Computer Science, Monash University (Dissertation) 1998, pp. 1-306.
	Schmidt, H. et al., "Behavioral synthesis for FPGA-based computing," Carnegie Mellon University, Pittsburgh, PA, 1994 IEEE, pp. 125-132.
	Schönfeld, M., et al., "The LISA Design Environment for the Synthesis of Array Processors Including Memories for the Data Transfer and Fault Tolerance by Reconfiguration and Coding Techniques," J. VLSI Signal Processing Systems for Signal, Image, and Video Technology, (1 October 1995) vol. 11(1/2), pp. 51-74
	Shin, D., et al., "C-based Interactive RTL Design Methodology," Technical Report CECS-03-42 (December 2003) pp. 1-16
	Singh, H. et al., "MorphoSys: An Integrated Reconfigurable System for Data-Parallel Computation-Intensive Applications," University of California, Irvine, CA. and Federal University of Rio de Janeiro, Brazil, 2000, IEEE Transactions on Computers, pp. 1-35.
	Sondervan, J., "Retiming and logic synthesis," Electronic Engineering (January 1993) vol. 65(793), pp.33, 35-36
	Soni, M., "VLSI Implementation of a Wormhole Run-time Reconfigurable Processor," June 2001, (Masters Thesis) Virginia Polytechnic Institute and State University, 88 pages.

INFORMATION DISCLOSURE STATEMENT BY APPLICANTS PTO-1449	Attorney Docket No. 2885/93	Serial No. 10/523,764
	Applicant(s) Vorbach et al.	
	Filing Date August 2, 2005	Group Art Unit 2187

EXAMINER'S INITIALS	AUTHOR, TITLE, DATE, PERTINENT PAGES, ETC.
	Sueyoshi, T, "Present Status and Problems of the Reconfigurable Computing Systems Toward the Computer Evolution," Department of Artificial Intelligence, Kyushu Institute of Technology, Fukuoka, Japan; Institute of Electronics, Information and Communication Engineers, Vol. 96, No. 426, IEICE Technical Report (1996), pp. 111-119 [English Abstract Only]
	Sutton et al., "A Multiprocessor DSP System Using PADDI-2," U.C. Berkeley, 1998 ACM, pp. 62-65.
	Tsutsui, A., et al., "YARDS: FPGA/MPU Hybrid Architecture for Telecommunication Data Processing," NTT Optical Network Systems Laboratories, Japan, 1997 ACM, pp. 93-99.
	Vasell et al., "The Function Processor: A Data-Driven Processor Array for Irregular Computations," Chalmers University of Technology, Sweden, pp. 1-21
	Waingold, E., et al., "Baring it all to software: Raw machines," IEEE Computer, September 1997, at 86-93
	Weinhardt, M., "Compilation Methods for Structure-programmable Computers," dissertation, ISBN 3-89722-011-3, 1997. [TABLE OF CONTENTS AND ENGLISH ABSTRACT PROVIDED]
	Weinhardt, Markus et al., "Pipeline Vectorization," IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, Vol. 20, No. 2, February 2001, pp. 234-248.
	Weinhardt, Markus et al., "Memory Access Optimization for Reconfigurable Systems," IEEE Proceedings Computers and Digital Techniques, 48(3) (May 2001) pp. 1-16.
	Wolfe, M. et al., "High Performance Compilers for Parallel Computing" (Addison-Wesley 1996) Table of Contents, 11 pages.
	XILINX, "Spartan and SpartanXL Families Field Programmable Gate Arrays," January 1999, Xilinx, pp. 4-3 through 4-70.
	XILINX, "XC6200 Field Programmable Gate Arrays," April 24, 1997, Xilinx product description, pp. 1-73.
	XILINX, "XC3000 Series Field Programmable Gate Arrays," November 6, 1998, Xilinx product description, pp. 1-76.
	XILINX, "XC4000E and XC4000X Series Field Programmable Gate Arrays," May 14, 1999, Xilinx product description, pp. 1-68.
	XILINX, "Virtex-E 1.8 V Extended Memory Field Programmable Gate Arrays," July 17, 2002, Xilinx Production Product Specification, pp. 1-118.
	XILINX, "Virtex-II and Virtex-II Pro X FPGA User Guide," March 28, 2007, Xilinx user guide, pp. 1-559.
	Zhang, et al., "A 1-V Heterogeneous Reconfigurable DSP IC for Wireless Baseband Digital Signal Processing," IEEE Journal of Solid-State Circuits, Vol. 35, No. 11, November 2000, pp. 1697-1704.
	Zhang et al., "Abstract: Low-Power Heterogeneous Reconfigurable Digital Signal Processors with Energy-Efficient Interconnect Network," U.C. Berkeley (2004), pp. 1-120.
	Zima, H. et al., "Supercompilers for parallel and vector computers" (Addison-Wesley 1991) Table of Contents, 5 pages.

EXAMINER	DATE CONSIDERED
EXAMINER: Initial if citation considered, whether or not citation is in conformance with M.P.E.P. 609; draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.	

INFORMATION DISCLOSURE STATEMENT BY APPLICANTS PTO-1449	Attorney Docket No. 2885/93	Serial No. 10/523,764
	Applicant(s) Vorbach et al.	
	Filing Date August 2, 2005	Group Art Unit 2187



U.S. PATENT DOCUMENTS

EXAMINER'S INITIALS	PATENT/ PUBLICATION NUMBER	PATENT/PUBLICATION DATE	NAME	CLASS	SUBCLASS	FILING DATE
	RE34,444	November 1993	Kaplinsky			
	RE37,195	May 29, 2001	Kean			
	4,414,547	November 1983	Knapp et al.			
	4,590,583	May 20, 1986	Miller			
	4,667,190	May 1987	Fant et al.			
	4,882,687	November 1989	Gordon			
	4,884,231	November 1980	Mor et al.			
	4,918,440	April 17, 1990	Furtek et al.			
	4,972,314	November 1990	Getzinger et al.			
	5,010,401	April 1991	Murakami et al.			
	5,034,914	July 1991	Osterlund			
	5,041,924	August 1991	Blackborow et al.			
	5,099,447	March 1992	Myszewski			
	5,193,202	March 1993	Jackson et al.			
	5,212,716	May 1993	Ferraiolo et al.			
	5,218,302	June 8, 1993	Loewe et al.			
	5,237,686	August 1993	Asano et al.			
	5,276,836	January 4, 1994	Fukumaru et al.			
	5,327,125	July 1994	Iwase et al.			
	5,343,406	Aug 30, 1994	Freeman et al.			
	5,418,953	May 1995	Hunt et al.			
	5,469,003	November 1995	Kean			
	5,537,580	July 1996	Giomi et al.			
	5,550,782	Aug 27, 1996	Cliff et al.			
	5,581,731	December 3, 1996	King et al.			
	5,625,836	Apr 29, 1997	Barker et al.			
	5,646,544	Jul 8, 1997	Iadanza			
	5,646,545	Jul 8, 1997	Trimberger et al.			
	5,652,529	July 1997	Gould et al.			
	5,737,565	April 1998	Mayfield			
	5,748,979	May 1998	Trimberger			
	5,752,035	May 1998	Trimberger			
	5,754,459	May 19, 1998	Telikapalli			
	5,754,820	May 19, 1998	Yamagami			
	5,781,756	Jul 14, 1998	Hung			
	5,781,756	Jul 14, 1998	Hung			
	5,801,547	September 1, 1998	Kean			
	5,801,958	September 1998	Dangelo et al.			

INFORMATION DISCLOSURE STATEMENT BY APPLICANTS PTO-1449	Attorney Docket No. 2885/93	Serial No. 10/523,764
	Applicant(s) Vorbach et al.	
	Filing Date August 2, 2005	Group Art Unit 2187

EXAMINER'S INITIALS	PATENT/ PUBLICATION NUMBER	PATENT/PUBLICATION DATE	NAME	CLASS	SUBCLASS	FILING DATE
	5,815,715	September 1998	Kayhan			
	5,821,774	October 1998	Veytsman et al.			
	5,831,448	Nov 3, 1998	Kean			
	5,844,422	December 1, 1998	Trimberger et al.			
	5,857,097	January 1999	Henninger et al.			
	5,862,403	January 1999	Kanai et al.			
	5,870,620	Feb 9, 1999	Kadosumi et al.			
	5,889,533	Mar 30, 1999	Lee			
	5,933,023	Aug 3, 1999	Young			
	5,960,193	September 28, 1999	Gutttag et al.			
	5,966,143	Oct 12, 1999	Breternitz, Jr.			
	5,978,583	November 1999	Ekanadham et al.			
	5,999,990	December 1999	Sharrit et al.			
	6,020,760	February 1, 2000	Sample et al.			
	6,026,481	February 2000	New et al.			
	6,044,030	Mar 28, 2000	Zheng et al.			
	6,077,315	June 2000	Greenbaum et a.			
	6,084,429	July 2000	Trimberger			
	6,105,106	August 2000	Manning			
	6,134,166	October 17, 2000	Lytle et al.			
	6,137,307	October 2000	Iwanczuk et al.			
	6,154,048	November 2000	Iwanczuk et al.			
	6,154,049	Nov 28, 2000	New			
	6,157,214	December 5, 2000	Marshall			
	6,185,256	February 2001	Saito et al.			
	6,185,731	February 2001	Macda et al.			
	6,188,240	February 2001	Nakaya			
	6,198,304	March 2001	Sasaki			
	6,201,406	March 2001	Iwanczuk et al.			
	6,204,687	March 2001	Schultz et al.			
	6,215,326	April 10, 2001	Jefferson et al.			
	6,216,223	April 2001	Revilla et al.			
	6,252,792	June 26, 2001	Marshall et al.			
	6,256,724	July 2001	Hocevar et al.			
	6,262,908	July 17, 2001	Marshall et al.			
	6,266,760	July 2001	DeHon et al.			
	6,285,624	September 2001	Chen			
	6,311,265	October 2001	Beckerle et al.			
	6,353,841	March 5, 2002	Marshall et al.			

INFORMATION DISCLOSURE STATEMENT BY APPLICANTS PTO-1449	Attorney Docket No. 2885/93	Serial No. 10/523,764
	Applicant(s) Vorbach et al.	
	Filing Date August 2, 2005	Group Art Unit 2187

EXAMINER'S INITIALS	PATENT/ PUBLICATION NUMBER	PATENT/PUBLICATION DATE	NAME	CLASS	SUBCLASS	FILING DATE
	6,362,650	Mar 26, 2002	New et al.			
	6,374,286	April 2002	Gec			
	6,373,779	Apr 16, 2002	Pang et al.			
	6,381,624	April 2002	Colon-Bonet et al.			
	6,400,601	June 2002	Sudo et al.			
	6,421,808	July 2002	McGeer			
	6,421,809	July 2002	Wuytack et al.			
	6,425,054	July 23, 2002	Nguyen			
	6,427,156	Jul 30, 2002	Chapman et al.			
	6,430,309	August 2002	Pressman et al.			
	6,434,642	Aug 13, 2002	Camilleri et al.			
	6,434,699	August 13, 2002	Jones et al.			
	6,435,054	October 10, 2000	Nguyen			
	6,438,747	August 2002	Schreiber et al.			
	6,476,634	November 2002	Bilski			
	6,487,709	November 2002	Keller et al.			
	6,490,695	December 2002	Zagorski et al.			
	6,507,947	January 2003	Schreiber et al.			
	6,516,382	February 2003	Manning			
	6,518,787	February 2003	Allegrucci et al.			
	6,523,107	February 18, 2003	Stansfield et al.			
	6,525,678	February 2003	Veenstra et al.			
	6,539,415	March 25, 2003	Mercs			
	6,539,438	March 25, 2003	Ledzius et al.			
	6,542,394	April 1, 2003	Marshall et al.			
	6,542,844	April 2003	Hanna			
	6,553,395	April 22, 2003	Marshall et al.			
	6,567,834	May 20, 2003	Marshall et al.			
	6,631,487	October 2003	Abramovici et al.			
	6,633,181	October 2003	Rupp			
	6,658,564	December 2003	Smith et al.			
	6,708,325	March 2004	Cooke et al.			
	6,754,805	June 2004	Yujen Juan			
	6,757,847	June 2004	Farkash et al.			
	6,757,892	June 2004	Gokhale et al.			

INFORMATION DISCLOSURE STATEMENT BY APPLICANTS PTO-1449	Attorney Docket No. 2885/93	Serial No. 10/523,764
	Applicant(s) Vorbach et al.	
	Filing Date August 2, 2005	Group Art Unit 2187

EXAMINER'S INITIALS	PATENT/ PUBLICATION NUMBER	PATENT/PUBLICATION DATE	NAME	CLASS	SUBCLASS	FILING DATE
	6,782,445	August 2004	Olgati et al.			
	6,785,826	August 31, 2004	Durham et al.			
	6,802,206	October 2004	Patterson et al.			
	6,803,787	October 2004	Wicker, Jr.			
	6,820,188	November 16, 2004	Stansfield et al.			
	6,829,697	December 2004	Davis et al.			
	6,847,370	January 2005	Baldwin et al.			
	6,871,341	March 2005	Shyr			
	6,874,108	March 2005	Abramovici et al.			
	6,886,092	April 2005	Douglass et al.			
	6,901,502	May 2005	Yano et al.			
	6,961,924	November 2005	Bates et al.			
	6,928,523	August 2005	Yamada, Akira			
	6,977,649	December 2005	Baldwin et al.			
	7,000,161	February 2006	Allen et al.			
	7,007,096	February 2006	Lisitsa et al.			
	7,010,687	March 2006	Ichimura			
	7,038,952	May 2, 2006	Zack et al.			
	7,210,129	April 2007	May et al.			
	7,237,087	June 26, 2007	Vorbach et al.			
	7,249,351	July 2007	Songer et al.			
	7,254,649	August 2007	Subramanian et al.			
	7,340,596	March 2008	Crosland et al.			
	7,350,178	March 2008	Crosland et al.			
	2001/001860	May 2001	Bieu			
	2001/010074	July 26, 2001	Nishihara et al.			
	2001/032305	October 2001	Barry			
	2002/083308	June 27, 2002	Pereira et al.			
	2002/103839	August 2002	Ozawa			
	2002/124238	September 05, 2002	Metzgen			
	2002/138716	September 26, 2002	Master et al.			
	2003/001615	January 2003	Sueyoshi et al.			
	2003/061542	March 2003	Bates et al.			
	2003/062922	Apr 3, 2003	Douglass et al.			
	2003/086300	May 2003	Noyes et al.			

INFORMATION DISCLOSURE STATEMENT BY APPLICANTS PTO-1449	Attorney Docket No. 2885/93	Serial No. 10/523,764
	Applicant(s) Vorbach et al.	
	Filing Date August 2, 2005	Group Art Unit 2187

EXAMINER'S INITIALS	PATENT/ PUBLICATION NUMBER	PATENT/PUBLICATION DATE	NAME	CLASS	SUBCLASS	FILING DATE
	2005/066213	March 2005	Vorbach et al.			
	2005/0144210	Jun 30, 2005	Simkins et al.			
	2005/0144212	Jun 30, 2005	Simkins et al.			
	2005/0144215	Jun 30, 2005	Simkins et al.			
	2006/0130096	Oct 12, 2006	Thendean et al.			
	2006/0230094	Oct 12, 2006	Simkins et al.			

FOREIGN PATENT DOCUMENTS

EXAMINER'S INITIALS	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATION	
						YES	NO
	0 398 552	November 22, 1990	EPO				
	0 746 106	December 4, 1996	EPO				
	1 061 439	December 20, 2000	EPO				
	1 669 885	Jun 14, 2006	EPO			Abstract	
	WO92/001987	February 6, 1992	PCT				
	WO98/010517	March 12, 1998	PCT				
	WO98/035294	August 13, 1998	PCT				
	WO00/049496	August 24, 2000	PCT				
	WO00/077652	December 21, 2000	PCT				
	WO02/050665	June 27, 2002	PCT				
	WO02/071196	September 12, 2002	PCT				
	WO04/114128	December 29, 2004	PCT				
	WO04/053718	June 24, 2004	PCT				
	WO05/045692	May 19, 2005	PCT				
	08069447	March 12, 1996	Japan			Abstract	
	2000-201066	July 18, 2000	Japan			Abstract	
	2001-500682	January 16, 2001	Japan			Abstract	
	05-509184	December 16, 2003	Japan			English Equivalent = USP 5,193,202 cited above	

OTHER DOCUMENTS

EXAMINER'S INITIALS	AUTHOR, TITLE, DATE, PERTINENT PAGES, ETC.
	Abnous et al., "Ultra-Low-Power Domain-Specific Multimedia Processors," U.C. Berkeley, 1996 IEEE, pp. 461-470.
	Albaharna, O.T. et al., "On the Viability of FPGA-Based Integrated Coprocessors," Dept. of Electrical and Electronic Engineering, Imperial College of Science, London, 1999 IEEE, pp. 206-215.
	Altera, "Flex 8000 Programmable Logic Device Family," Altera Corporation product description, January 2003, pp. 1-62.

INFORMATION DISCLOSURE STATEMENT BY APPLICANTS PTO-1449	Attorney Docket No. 2885/93	Serial No. 10/523,764
	Applicant(s) Vorbach et al.	
	Filing Date August 2, 2005	Group Art Unit 2187

EXAMINER'S INITIALS	AUTHOR, TITLE, DATE, PERTINENT PAGES, ETC.
	Altera, "Flex 10K Embedded Programmable Logic Device Family," Altera Corporation product description, January 2003, pp. 1-128.
	Athanas et al., "Processor Reconfiguration Through Instruction-Set Metamorphosis," 1993, IEEE Computers, pp. 11-18.
	Atmel, 5-K-50K Gates Coprocessor FPGA with Free Ram, Data Sheet, July 2006, 55 pages.
	Atmel, FPGA-based FIR Filter Application Note, September 1999, 10 pages.
	Atmel, "An Introduction to DSP Applications using the AT40K FPGA," FPGA Application Engineering, San Jose, CA, April 2004, 15 pages.
	Atmel, Configurable Logic Design & Application Book, Atmel Corporation, 1995, pp. 2-19 through 2-25.
	Atmel, Field Programmable Gate Array Configuration Guide, AT6000 Series Configuration Data Sheet, September 1999, pp. 1-20.
	Bacon, D. et al., "Compiler Transformations for High-Performance Computing," ACM Computing Surveys, 26(4):325-420 (1994)
	Bakkes, P.J., et al., "Mixing Fixed and Reconfigurable Logic for Array Processing," Dept. of Electrical and Electronic Engineering, University of Stellenbosch, South Africa, 1996 IEEE, pp. 118-125.
	Beck et al., "From control flow to data flow," TR 89-1050, October 1989, Dept. of Computer Science, Cornell University, Ithaca, NY, pp. 1-25.
	Becker, J. et al., "Architecture, Memory and Interface Technology Integration of an Industrial/Academic Configurable System-on-Chip (CSoC)," IEEE Computer Society Annual Workshop on VLSI (WVLSI 2003), (February 2003)
	Becker, J., "Configurable Systems-on-Chip (CSoC)," (Invited Tutorial), Proc. of 9th Proc. of XV Brazilian Symposium on Integrated Circuit, Design (SBCCI 2002), (September 2002)
	Becker et al., "Automatic Parallelism Exploitation for FPL-Based Accelerators." 1998, Proc. 31 st Annual Hawaii International Conference on System Sciences, pp. 169-178.
	Bratt, A., "Motorola field programmable analogue arrays, present hardware and future trends," Motorola Programmable Technology Centre, Gadbroke Business Centre, Northwich, Cheshire, 1998, The Institute of Electrical Engineers, IEE, Savoy Place, London, pp. 1-5.
	Cardoso, J.M.P. et al., "A novel algorithm combining temporal partitioning and sharing of functional units," University of Algarve, Faro, Portugal, 2001 IEEE, pp. 1-10.
	Cardoso, Joao M.P. and Markus Weinhardt, "XPP-VC: A C Compiler with Temporal Partitioning for the PACT-XPP Architecture," Field-Programmable Logic and Applications. Reconfigurable Computing is Going Mainstream, 12 th International Conference FPL 2002, Proceedings (Lecture Notes in Computer Science, Vol. 2438) Springer-Verlag Berlin, Germany, 2002, pp. 864-874.
	Cardoso, J.M.P. et al., "Compilation and Temporal Partitioning for a Coarse-Grain Reconfigurable Architecture," LYSACHT, P. & ROSENTIEL, W. eds., "New Algorithms, Architectures and Applications for Reconfigurable Computing," (2005) pp. 105-115
	Cardoso, J.M.P. et al., "Macro-Based Hardware Compilation of Java™ Bytecodes into a Dynamic Reconfigurable Computing System," Field-Programmable Custom Computing Machines (1999) FCCM '99. Proceedings. Seventh Annual IEEE Symposium on NAPA Valley, CA, USA, 21-23 April 1999, IEEE Comput. Soc, US, (21 April 1999) pp.2-11
	Clearspeed, CSX Processor Architecture, Whitepaper, PN-1110-0702, 2007, pp. 1-15, www.clearspeed.com .
	Clearspeed, CSX Processor Architecture, Whitepaper, PN-1110-0306, 2006, pp. 1-14, www.clearspeed.com .
	Compton, K. et al., "Configurable Computing: A Survey of Systems and Software," Northwestern University, Dept. of ECE, Technical Report, 1999, (XP-002315148), 39 pages.
	Cook, Jeffrey J., "The Amalgam Compiler Infrastructure," Thesis at the University of Illinois at Urbana-Champaign (2004) Chapter 7 & Appendix G
	Cronquist, D. et al., "Architecture Design of Reconfigurable Pipelined Datapaths," Department of Computer Science and Engineering, University of Washington, Seattle, WA, Proceedings of the 20 th Anniversary Conference on Advanced Research in VLSI, 1999, pp. 1-15.
	DeHon, A., "DPGA Utilization and Application," MIT Artificial Intelligence Laboratory, Proceedings of the Fourth International ACM Symposium on Field-Programmable Gate Arrays (FPGA '96), IEEE Computer Society, pp. 1-7.
	DeHon, Andre, "Reconfigurable Architectures for General-Purpose Computing," Massachusetts Institute of Technology, Technical Report AITR-1586, October 1996 (1996-10), XP002445054, Cambridge, MA, pp. 1-353.

INFORMATION DISCLOSURE STATEMENT BY APPLICANTS PTO-1449	Attorney Docket No. 2885/93	Serial No. 10/523,764
	Applicant(s) Vorbach et al.	
	Filing Date August 2, 2005	Group Art Unit 2187

EXAMINER'S INITIALS	AUTHOR, TITLE, DATE, PERTINENT PAGES, ETC.
	Diniz, P., et al., "A behavioral synthesis estimation interface for configurable computing," University of Southern California, Marina Del Rey, CA, 2001 IEEE, pp. 1-2.
	Ebeling, C. et al., "Mapping Applications to the RaPiD Configurable Architecture," Department of Computer Science and Engineering, University of Washington, Seattle, WA, <i>FPGAs for Custom Computing Machines</i> , 1997. Proceedings., The 5th Annual IEEE Symposium, Publication Date: 16-18 Apr 1997, 10 pages.
	Equator, Pixels to Packets, Enabling Multi-Format High Definition Video, Equator Technologies BSP-15 Product Brief, www.equator.com , 2001, 4 pages.
	Fawcett, B.K., "Map, Place and Route: The Key to High-Density PLD Implementation," Wescon Conference, IEEE Center (7 November 1995) pp. 292-297
	Franklin, Manoj et al., "A Fill-Unit Approach to Multiple Instruction Issue," Proceedings of the Annual International Symposium on Microarchitecture, November 1994, pp. 162-171.
	Freescall Slide Presentation, An Introduction to Motorola's RCF (Reconfigurable Compute Fabric) Technology, Presented by Frank David, Launched by Freescall Semiconductor, Inc., 2004, 39 pages.
	Genius, D. et al., "A Case for Array Merging in Memory Hierarchies," Proceedings of the 9th International Workshop on Compilers for Parallel Computers, CPC'01 (June 2001), 10 pages.
	Hartenstein, R. et al., "A new FPGA architecture for word-oriented datapaths," Proc. FPL'94, Springer LNCS, September 1994, pp. 144-155.
	Hartenstein, R., "Coarse grain reconfigurable architectures," Design Automation Conference, 2001, Proceedings of the ASP-DAC 2001 Asia and South Pacific, January 30- February 2, 2001, IEEE 30 January 2001, pp. 564-569.
	Hendrich, N., et al., "Silicon Compilation and Rapid Prototyping of Microprogrammed VLSI-Circuits with MIMOLA and SOLO 1400," Microprocessing & Microprogramming (September 1992) vol.35(1-5), pp. 287-294
	Hwang, K., "Advanced Computer Architecture - Parallelism, Scalability, Programmability," 1993, McGraw-Hill, Inc., pp. 348-355.
	Hwang, K., "Computer Architecture and Parallel Processing," Data Flow Computers and VLSI Computations, XP-002418655, 1985 McGraw-Hill, Chapter 10, pp. 732-807.
	IBM Technical Disclosure Bulletin, IBM Corp., New York, XP000424878, Bd. 36, Nr. 11, 1 November 1993, pp. 335-336.
	Inside DSP, "Ambric Discloses Massively Parallel Architecture," August 23, 2006, HTTP://insidedsp.com/tabid/64/articleType/ArticleView/articleId/155/Defa... , 2 pages.
	Intel, Intel MXP5800/MXP5400 Digital Media Processors, Architecture Overview, June 2004, Revision 2.4, pp. 1-24.
	Kaul, M., et al., "An automated temporal partitioning and loop fission approach of FPGA based reconfigurable synthesis of DSP applications," University of Cincinnati, Cincinnati, OH, ACM 1999, pp. 616-622.
	Kean, T.A., "Configurable Logic: A Dynamically Programmable Cellular Architecture and its VLSI Implementation," University of Edinburgh (Dissertation) 1988, pp. 1-286
	Kean, T., et al., "A Fast Constant Coefficient Multiplier for the XC6200," Xilinx, Inc., Lecture Notes in Computer Science, Vol. 1142, Proceedings of the 6 th International Workshop of Field-Programmable Logic, 1996, 7 pages.
	Kim et al., "A Reconfigurable Multifunction Computing Cache Architecture," IEEE Transactions on Very Large Scale Integration (VLSI) Systems Volume 9, Issue 4, Aug 2001 Page(s):509 - 523.
	Knittel, Gunter, "A PCI-compatible FPGA-Coprocessor for 2D/3D Image Processing," University of Turgingen, Germany, 1996 IEEE, pp. 136-145.
	Koch, Andreas et al., "High-Level-Language Compilation for Reconfigurable Computers," Proceedings of European Workshop on Reconfigurable Communication-Centric SOCS (June 2005) 8 pages
	Koren et al., "A data-driven VLSI array for arbitrary algorithms," IEEE Computer Society, Long Beach, CA Vol. 21, No. 10, 1 October 1988, pp. 30-34.
	Larsen, S. et al., "Increasing and Detecting Memory Address Congruence," Proceedings of the 2002 IEEE International Conference on Parallel Architectures and Compilation Techniques (PACT'02), pp. 1-12 (September 2002).
	Lee et al., "A new distribution network based on controlled switching elements and its applications," IEEE/ACT Trans. of Networking, Vol. 3, No. 1, pp. 70-81, February 1995.
	Lee, Jong-eun et al., "Reconfigurable ALU Array Architecture with Conditional Execution," International Soc. Design Conference (ISOOC) [online] October 25, 2004, Seoul, Korea, 5 pages.

INFORMATION DISCLOSURE STATEMENT BY APPLICANTS PTO-1449	Attorney Docket No. 2885/93	Serial No. 10/523,764
	Applicant(s) Vorbach et al.	
	Filing Date August 2, 2005	Group Art Unit 2187

EXAMINER'S INITIALS	AUTHOR, TITLE, DATE, PERTINENT PAGES, ETC.
	Ling, X., "WASMII: An MPLD with Data-Driven Control on a Virtual Hardware," Journal of Supercomputing, Kluwer Academic Publishers, Dordrecht, Netherlands, 1995, pp. 253-276.
	Ling et al., "WASMII: A Multifunction Programmable Logic Device (MPLD) with Data Driven Control," The Transactions of the Institute of Electronics, Information and Communication Engineers, 25 April 1994, Vol. J77-D-1, Nr. 4, pp. 309-317. [This references is in Chinese, but should be comparable in content to the Ling et al. reference above]
	Margolus, N., "An FPGA architecture for DRAM-based systolic computations," Boston University Center for Computational Science and MIT Artificial Intelligence Laboratory, IEEE 1997, pp. 2-11.
	Mei, Bingfeng, "A Coarse-Grained Reconfigurable Architecture Template and Its Compilation Techniques," Katholieke Universiteit Leuven, PhD Thesis, January 2005, IMEC vzw, Universitair Micro-Electronica Centrum, Belgium, pp. 1-195 (and Table of Contents).
	Mei, Bingfeng, et al., "Design and Optimization of Dynamically Reconfigurable Embedded Systems," IMEC vzw, 2003, Belgium, 7 pages, http://www.imec.be/reconfigurable/pdf/ICERSA_01_design.pdf .
	Miyamori, T. et al., "REMARC: Reconfigurable Multimedia Array Coprocessor," Computer Systems Laboratory, Stanford University, IEICE TRANSACTIONS ON INFORMATION AND SYSTEMS E SERIES D, 1999; (abstract): Proceedings of the 1998 ACM/SIGDA sixth international symposium on Field programmable gate arrays, p.261, February 22-25, 1998, Monterey, California, United States, pp. 1-12.
	Moracs, F., et al., "A Physical Synthesis Design Flow Based on Virtual Components," XV Conference on Design of Circuits and Integrated Systems (November 2000) 6 pages
	Muchnick, S., "Advanced Compiler Design and Implementation" (Morgan Kaufmann 1997), Table of Contents, 11 pages
	Murphy, C., "Virtual Hardware Using Dynamic Reconfigurable Field Programmable Gate Arrays," Engineering Development Centre, Liverpool John Moores University, UK, GERI Annual Research Symposium 2005, 8 pages.
	Nageldinger, U., "Design-Space Exploration for Coarse Grained Reconfigurable Architectures," (Dissertation) Universitaet Kaiserslautern, 2000, Chapter 2, pp. 19-45.
	Neumann, T., et al., "A Generic Library for Adaptive Computing Environments," Field Programmable Logic and Applications, 11 th International Conference, FPL 2001, Proceedings (Lecture Notes in Computer Science, vol. 2147) (2001) pp. 503-512
	Olukotun, K., "The Case for a Single-Chip Microprocessor," ACM Sigplan Notices, ACM, Association for Computing Machinery, New York, Vol. 31, No. 9, September 1996 (1996-09-00) pp. 2-11.
	Ozawa, Motokazu et al., "A Cascade ALU Architecture for Asynchronous Super-Scalar Processors," IEICE Transactions on Electronics, Electronics Society, Tokyo, Japan, Vol. E84-C, No. 2, February 2001, pp. 229-237.
	PACT Corporation, "The XPP Communication System," Technical Report 15 (2000), pp. 1-16.
	Quenot, G.M., et al., "A Reconfigurable Compute Engine for Real-Time Vision Automata Prototyping," Laboratoire Systeme de Perception, DGA/Etablissement Technique Central de l'Armement, France, 1994 IEEE, pp. 91-100.
	Parhami, B., "Parallel Counters for Signed Binary Signals," Signals, Systems and Computers, 1989, Twenty-Third Asilomar Conference, Volume 1, pp. 513-516.
	Saleeba, Z.M.G., "A Self-Reconfiguring Computer System," Department of Computer Science, Monash University (Dissertation) 1998, pp. 1-306.
	Schmidt, H. et al., "Behavioral synthesis for FPGA-based computing," Carnegie Mellon University, Pittsburgh, PA, 1994 IEEE, pp. 125-132.
	Schönfeld, M., et al., "The LISA Design Environment for the Synthesis of Array Processors Including Memories for the Data Transfer and Fault Tolerance by Reconfiguration and Coding Techniques," J. VLSI Signal Processing Systems for Signal, Image, and Video Technology, (1 October 1995) vol. 11(1/2), pp. 51-74
	Shin, D., et al., "C-based Interactive RTL Design Methodology," Technical Report CECS-03-42 (December 2003) pp. 1-16
	Singh, H. et al., "MorphoSys: An Integrated Reconfigurable System for Data-Parallel Computation-Intensive Applications," University of California, Irvine, CA. and Federal University of Rio de Janeiro, Brazil, 2000, IEEE Transactions on Computers, pp. 1-35.
	Sondervan, J., "Retiming and logic synthesis," Electronic Engineering (January 1993) vol. 65(793), pp.33, 35-36
	Soni, M., "VLSI Implementation of a Wormhole Run-time Reconfigurable Processor," June 2001, (Masters Thesis) Virginia Polytechnic Institute and State University, 88 pages.

DUPLICATION

INFORMATION DISCLOSURE STATEMENT BY APPLICANTS PTO-1449	Attorney Docket No. 2885/93	Serial No. 10/523,764
	Applicant(s) Vorbach et al.	
	Filing Date August 2, 2005	Group Art Unit 2187

EXAMINER'S INITIALS	AUTHOR, TITLE, DATE, PERTINENT PAGES, ETC.
	Sueyoshi, T, "Present Status and Problems of the Reconfigurable Computing Systems Toward the Computer Evolution," Department of Artificial Intelligence, Kyushu Institute of Technology, Fukuoka, Japan; Institute of Electronics, Information and Communication Engineers, Vol. 96, No. 426, IEICE Technical Report (1996), pp. 111-119 [English Abstract Only]
	Sutton et al., "A Multiprocessor DSP System Using PADDI-2," U.C. Berkeley, 1998 ACM, pp. 62-65.
	Tsutsui, A., et al., "YARDS: FPGA/MPU Hybrid Architecture for Telecommunication Data Processing," NTT Optical Network Systems Laboratories, Japan, 1997 ACM, pp. 93-99.
	Vasell et al., "The Function Processor: A Data-Driven Processor Array for Irregular Computations," Chalmers University of Technology, Sweden, pp. 1-21
	Waingold, E., et al., "Baring it all to software: Raw machines," IEEE Computer, September 1997, at 86-93
	Weinhardt, M., "Compilation Methods for Structure-programmable Computers," dissertation, ISBN 3-89722-011-3, 1997. [TABLE OF CONTENTS AND ENGLISH ABSTRACT PROVIDED]
	Weinhardt, Markus et al., "Pipeline Vectorization," IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, Vol. 20, No. 2, February 2001, pp. 234-248.
	Weinhardt, Markus et al., "Memory Access Optimization for Reconfigurable Systems," IEEE Proceedings Computers and Digital Techniques, 48(3) (May 2001) pp. 1-16.
	Wolfe, M. et al., "High Performance Compilers for Parallel Computing" (Addison-Wesley 1996) Table of Contents, 11 pages.
	XILINX, "Spartan and SpartanXL Families Field Programmable Gate Arrays," January 1999, Xilinx, pp. 4-3 through 4-70.
	XILINX, "XC6200 Field Programmable Gate Arrays," April 24, 1997, Xilinx product description, pp. 1-73.
	XILINX, "XC3000 Series Field Programmable Gate Arrays," November 6, 1998, Xilinx product description, pp. 1-76.
	XILINX, "XC4000E and XC4000X Series Field Programmable Gate Arrays," May 14, 1999, Xilinx product description, pp. 1-68.
	XILINX, "Virtex-E 1.8 V Extended Memory Field Programmable Gate Arrays," July 17, 2002, Xilinx Production Product Specification, pp. 1-118.
	XILINX, "Virtex-II and Virtex-II Pro X FPGA User Guide," March 28, 2007, Xilinx user guide, pp. 1-559.
	Zhang, et al., "A 1-V Heterogeneous Reconfigurable DSP IC for Wireless Baseband Digital Signal Processing," IEEE Journal of Solid-State Circuits, Vol. 35, No. 11, November 2000, pp. 1697-1704.
	Zhang et al., "Abstract: Low-Power Heterogeneous Reconfigurable Digital Signal Processors with Energy-Efficient Interconnect Network," U.C. Berkeley (2004), pp. 1-120.
	Zima, H. et al., "Supercompilers for parallel and vector computers" (Addison-Wesley 1991) Table of Contents, 5 pages.

EXAMINER	DATE CONSIDERED
<p>EXAMINER: Initial if citation considered, whether or not citation is in conformance with M.P.E.P. 609; draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.</p>	